

RF Power LDMOS Transistor

N-Channel Enhancement-Mode Lateral MOSFET

Designed for Class A or Class AB power amplifier applications with frequencies up to 2000 MHz. Suitable for analog and digital modulation and multicarrier amplifier applications.

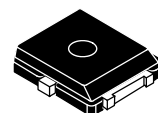
- Typical Two-Tone Performance @ 1960 MHz, 28 Vdc, $I_{DQ} = 50$ mA,
 $P_{out} = 4$ W PEP
 Power Gain — 18 dB
 Drain Efficiency — 33%
 IMD — -34 dBc
- Typical Two-Tone Performance @ 900 MHz, 28 Vdc, $I_{DQ} = 50$ mA,
 $P_{out} = 4$ W PEP
 Power Gain — 19 dB
 Drain Efficiency — 33%
 IMD — -39 dBc
- Capable of Handling 5:1 VSWR @ 28 Vdc, 1960 MHz, 4 W CW Output Power

Features

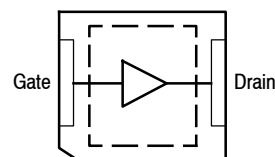
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- On-Chip RF Feedback for Broadband Stability
- Integrated ESD Protection
- In Tape and Reel. T1 Suffix = 1,000 Units, 16 mm Tape Width, 7-inch Reel.

MMRF1014NT1

**1-2000 MHz, 4 W, 28 V
CLASS A/AB
RF POWER MOSFET**



**PLD-1.5
PLASTIC**



Note: The center pad on the backside of the package is the source terminal for the transistor.

Figure 1. Pin Connections

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +68	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +12	Vdc
Storage Temperature Range	T_{stg}	- 65 to +150	°C
Operating Junction Temperature	T_J	150	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (1,2)	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.8	°C/W
Case Temperature 76°C, 4 W PEP, Two-Tone		8.5	
Case Temperature 79°C, 4 W CW			

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1C
Machine Model (per EIA/JESD22-A115)	A
Charge Device Model (per JESD22-C101)	IV

1. MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
2. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1955.

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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Off Characteristics

Zero Gate Voltage Drain Leakage Current ($V_{DS} = 68\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 28\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	10	μAdc
Gate-Source Leakage Current ($V_{GS} = 5\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	—	—	500	nAdc

On Characteristics

Gate Threshold Voltage ($V_{DS} = 10\text{ Vdc}$, $I_D = 50\text{ mAdc}$)	$V_{GS(th)}$	1.2	2	2.7	Vdc
Gate Quiescent Voltage ($V_{DS} = 28\text{ Vdc}$, $I_D = 50\text{ mAdc}$)	$V_{GS(Q)}$	—	2.7	—	Vdc
Fixture Gate Quiescent Voltage ⁽¹⁾ ($V_{DD} = 28\text{ Vdc}$, $I_D = 50\text{ mAdc}$, Measured in Functional Test)	$V_{GG(Q)}$	2.2	3	4.2	Vdc
Drain-Source On-Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 50\text{ mAdc}$)	$V_{DS(on)}$	—	0.27	0.37	Vdc

Dynamic Characteristics

Reverse Transfer Capacitance ($V_{DS} = 28\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$)	C_{rss}	—	21	—	pF
Output Capacitance ($V_{DS} = 28\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$)	C_{oss}	—	25	—	pF
Input Capacitance ($V_{DS} = 28\text{ Vdc}$, $V_{GS} = 0\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz)	C_{iss}	—	30	—	pF

Functional Tests (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $I_{DQ} = 50\text{ mA}$, $P_{out} = 4\text{ W PEP}$, $f_1 = 1960\text{ MHz}$, $f_2 = 1960.1\text{ MHz}$, Two-Tone Test

Power Gain	G_{ps}	16.5	18	20	dB
Drain Efficiency	η_D	28	33	—	%
Intermodulation Distortion	IMD	—	-34	-28	dBc
Input Return Loss	IRL	—	-12	-10	dB

Typical Performance (In Freescale 900 MHz Demo Board, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $I_{DQ} = 50\text{ mA}$, $P_{out} = 4\text{ W PEP}$, $f = 900\text{ MHz}$, Two-Tone Test, 100 kHz Tone Spacing

Power Gain	G_{ps}	—	19	—	dB
Drain Efficiency	η_D	—	33	—	%
Intermodulation Distortion	IMD	—	-39	—	dBc
Input Return Loss	IRL	—	-12	—	dB

1. $V_{GG} = \frac{11}{10} \times V_{GS(Q)}$. Parameter measured on Freescale Test Fixture, due to resistive divider network on the board. Refer to Test Circuit Schematic.

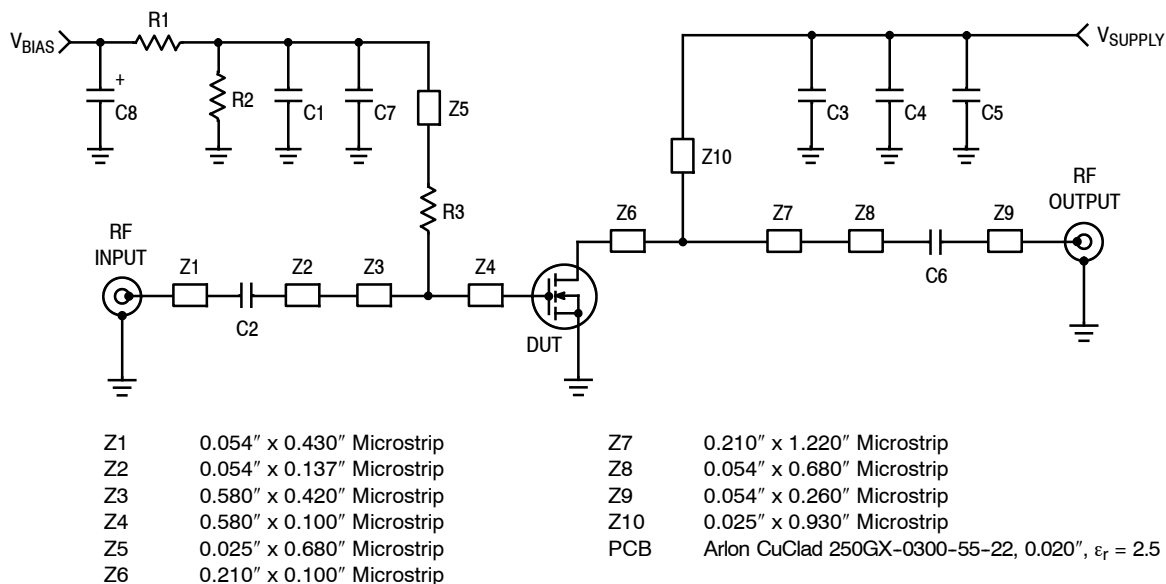


Figure 2. MMRF1014NT1 Test Circuit Schematic

Table 6. MMRF1014NT1 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1	100 nF Chip Capacitor	CDR33BX104AKYS	Kemet
C2, C3, C6, C7	9.1 pF Chip Capacitors	ATC100B9R1CT500XT	ATC
C4, C5	10 μ F, 50 V Chip Capacitors	GRM55DR61H106KA88B	Murata
C8	10 μ F, 35 V Tantalum Chip Capacitor	T490D106K035AT	Kemet
R1	1 k Ω , 1/4 W Chip Resistor	CRCW12061001FKEA	Vishay
R2	10 k Ω , 1/4 W Chip Resistor	CRCW12061002FKEA	Vishay
R3	10 Ω , 1/4 W Chip Resistor	CRCW120610R0FKEA	Vishay

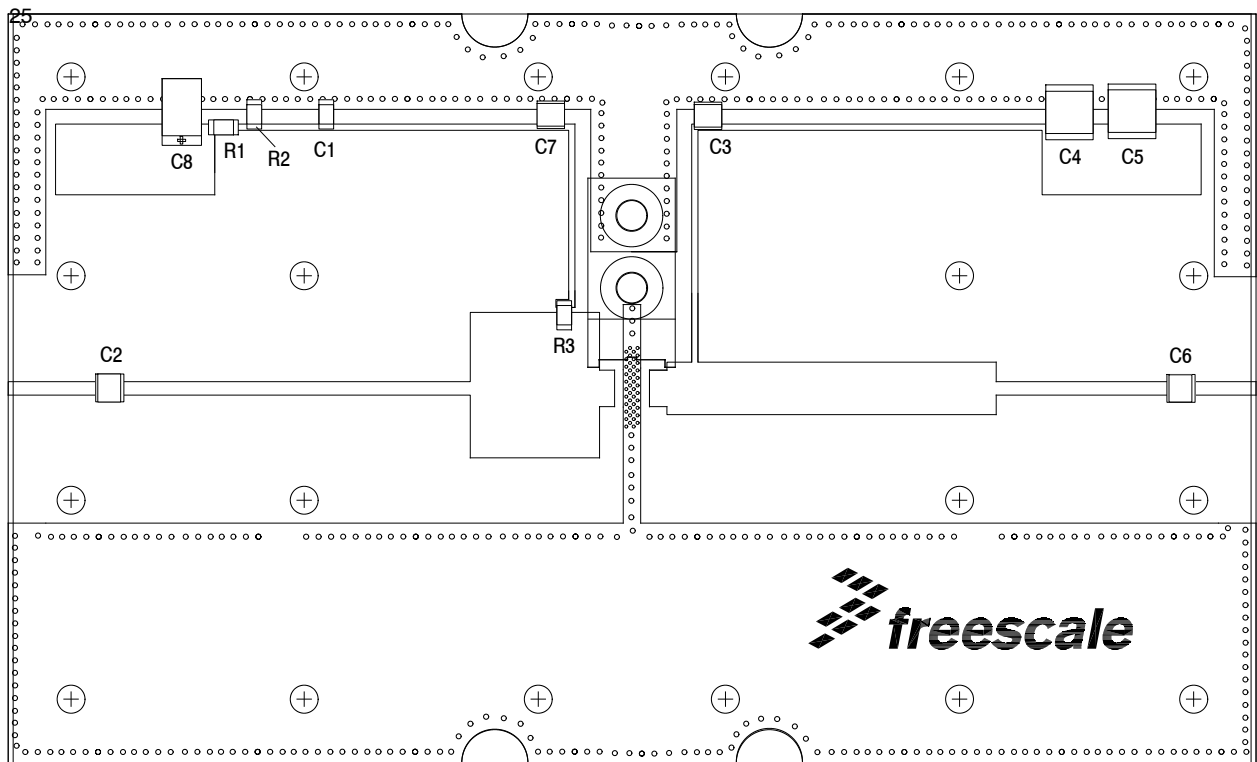
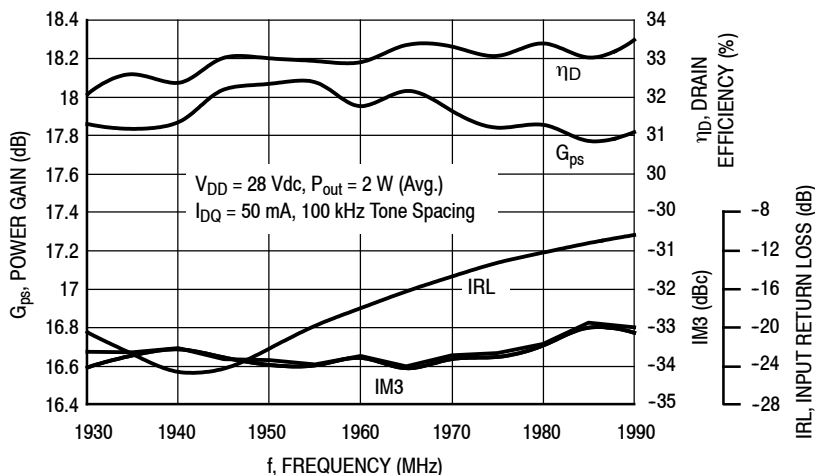
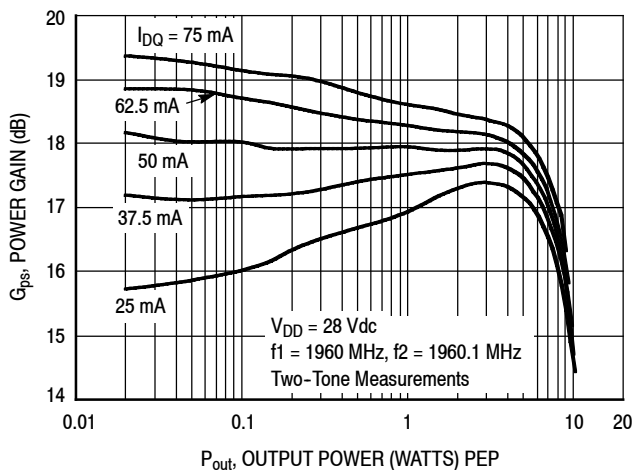


Figure 3. MMRF1014NT1 Test Circuit Component Layout

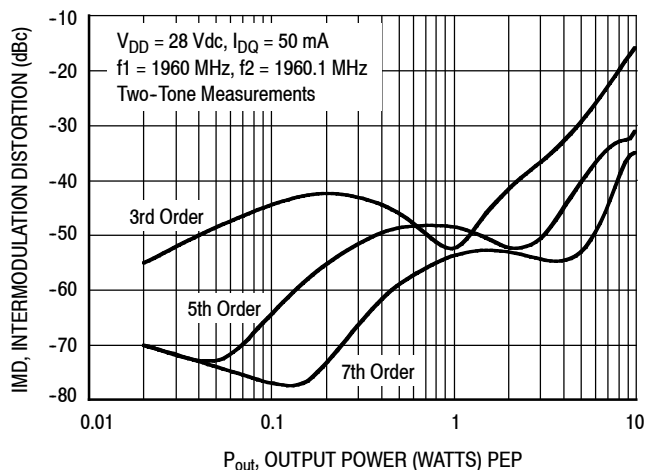
TYPICAL CHARACTERISTICS



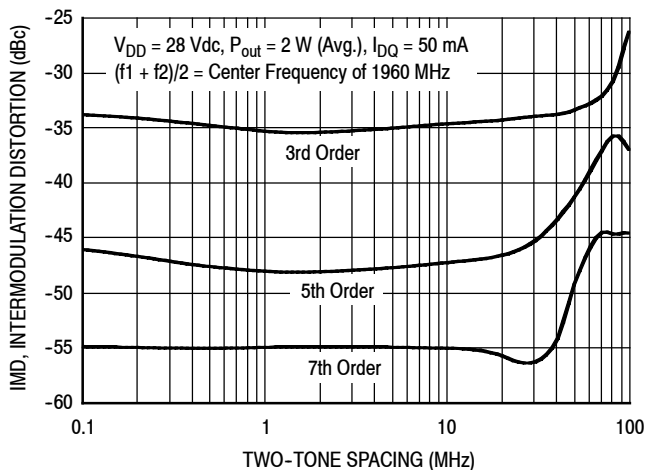
**Figure 4. Two-Tone Wideband Performance
@ $P_{out} = 2 \text{ Watts Avg.}$**



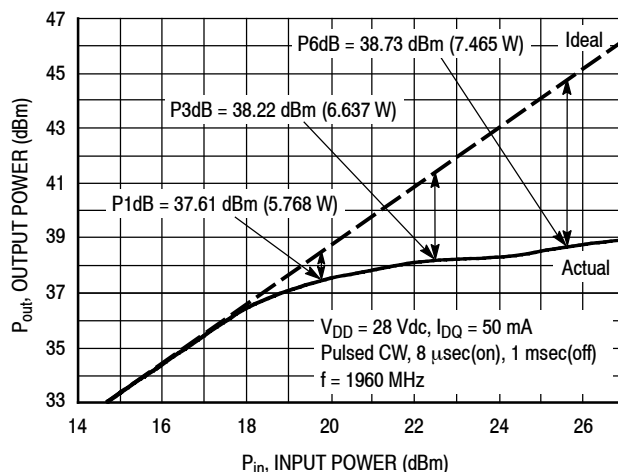
**Figure 5. Two-Tone Power Gain versus
Output Power**



**Figure 6. Intermodulation Distortion Products
versus Output Power**



**Figure 7. Intermodulation Distortion Products
versus Tone Spacing**



**Figure 8. Pulsed CW Output Power versus
Input Power**

TYPICAL CHARACTERISTICS

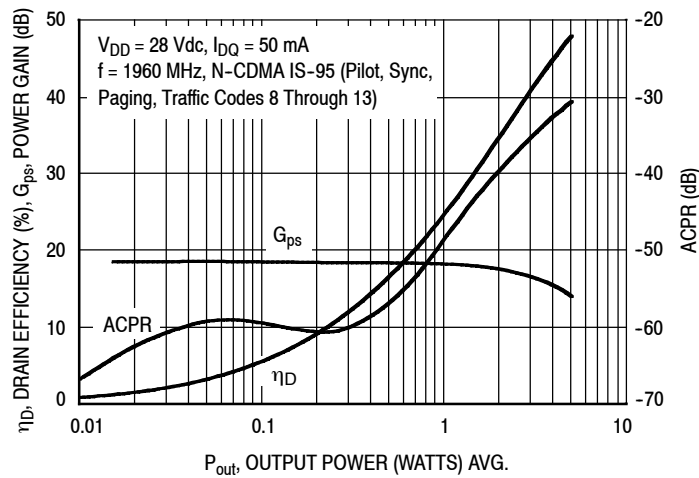


Figure 9. Single-Carrier CDMA ACPR, Power Gain and Drain Efficiency versus Output Power

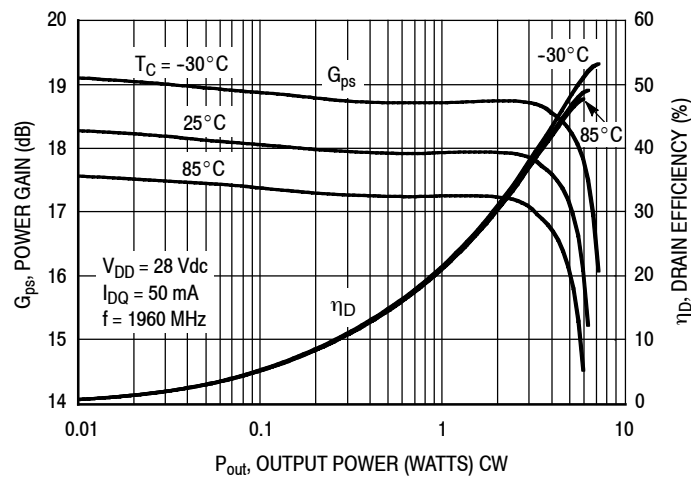


Figure 10. Power Gain and Drain Efficiency versus CW Output Power

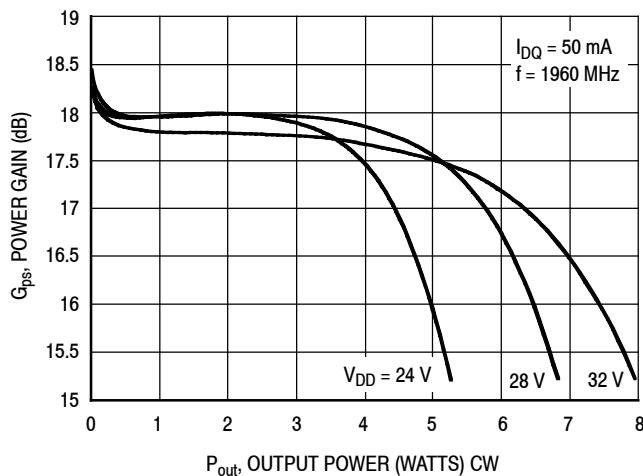


Figure 11. Power Gain versus Output Power

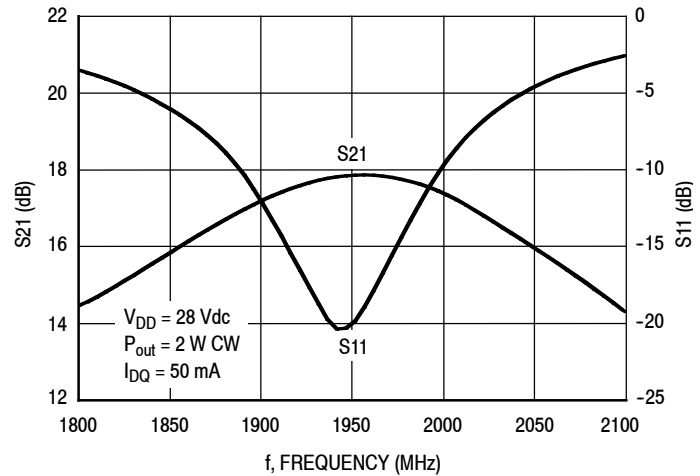
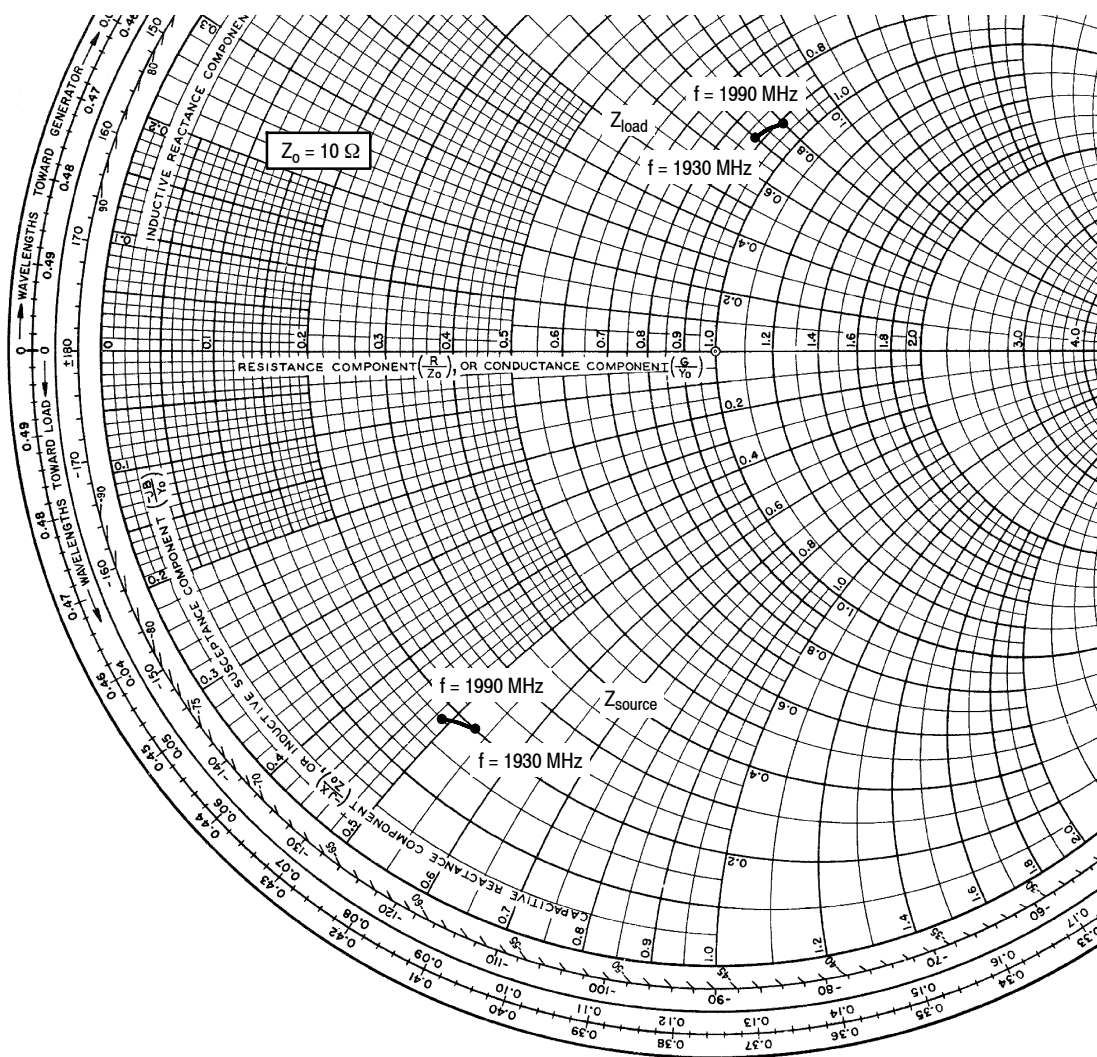


Figure 12. Broadband Frequency Response



$V_{DD} = 28 \text{ Vdc}$, $I_{DQ} = 50 \text{ mA}$, $P_{\text{out}} = 4 \text{ W PEP}$

f MHz	Z_{source} Ω	Z_{load} Ω
1930	$1.96 - j5.34$	$8.78 + j6.96$
1960	$1.89 - j5.10$	$8.93 + j7.46$
1990	$1.82 - j4.85$	$9.11 + j7.97$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

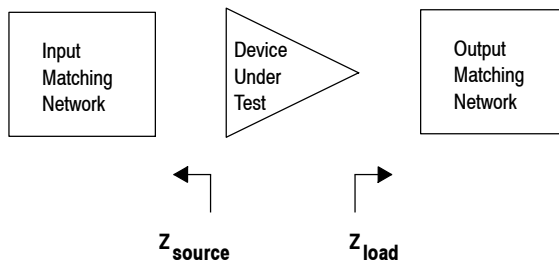


Figure 13. Series Equivalent Source and Load Impedance

Table 7. Common Source S-Parameters ($V_{DD} = 28 \text{ Vdc}$, $I_{DQ} = 50 \text{ mA}$, $T_A = 25^\circ\text{C}$, 50 Ohm System)

f MHz	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	S ₁₁	∠ φ	S ₂₁	∠ φ	S ₁₂	∠ φ	S ₂₂	∠ φ
500	0.649	-116.340	7.902	105.420	0.056	-73.750	0.548	-33.570
550	0.695	-121.680	7.502	98.790	0.053	-80.570	0.593	-41.480
600	0.733	-126.560	7.111	92.380	0.049	-87.010	0.632	-48.890
650	0.770	-131.340	6.699	86.290	0.045	-93.280	0.669	-56.000
700	0.800	-135.740	6.302	80.450	0.041	-99.120	0.701	-62.810
750	0.827	-140.030	5.922	74.850	0.038	-104.850	0.727	-69.290
800	0.848	-143.950	5.552	69.630	0.035	-110.110	0.750	-75.350
850	0.866	-147.690	5.220	64.580	0.032	-115.220	0.770	-81.130
900	0.882	-151.140	4.891	59.970	0.029	-119.960	0.786	-86.570
950	0.895	-154.560	4.597	55.490	0.026	-124.790	0.800	-91.730
1000	0.907	-157.590	4.315	51.240	0.024	-129.090	0.813	-96.660
1050	0.916	-160.540	4.060	47.170	0.022	-133.370	0.824	-101.340
1100	0.923	-163.310	3.819	43.340	0.020	-137.460	0.833	-105.790
1150	0.929	-165.930	3.601	39.650	0.018	-141.440	0.840	-110.050
1200	0.935	-168.430	3.398	36.110	0.017	-145.330	0.847	-114.170
1250	0.938	-170.770	3.210	32.740	0.015	-149.540	0.851	-118.060
1300	0.942	-173.030	3.036	29.490	0.014	-153.430	0.856	-121.880
1350	0.945	-175.140	2.875	26.360	0.013	-157.460	0.859	-125.520
1400	0.948	-177.170	2.728	23.330	0.012	-161.910	0.863	-129.020
1450	0.951	-179.090	2.590	20.440	0.011	-166.180	0.866	-132.390
1500	0.953	-179.030	2.464	17.640	0.010	-170.630	0.869	-135.650
1550	0.954	-177.270	2.347	14.920	0.009	-174.890	0.872	-138.760
1600	0.955	-175.570	2.240	12.320	0.008	-179.950	0.875	-141.750
1650	0.956	-173.980	2.139	9.740	0.008	-173.920	0.877	-144.650
1700	0.957	-172.350	2.047	7.250	0.007	-167.710	0.880	-147.480
1750	0.957	-170.800	1.958	4.810	0.007	-161.810	0.882	-150.180
1800	0.958	-169.340	1.879	2.440	0.006	-155.370	0.884	-152.760
1850	0.959	-167.920	1.806	0.260	0.006	-148.940	0.886	-155.230
1900	0.959	-166.510	1.736	-1.980	0.005	-142.630	0.887	-157.580
1950	0.960	-165.200	1.668	-4.310	0.005	-136.740	0.888	-160.050
2000	0.959	-163.800	1.611	-6.240	0.005	-129.910	0.890	-162.070
2050	0.959	-162.420	1.555	-8.290	0.005	-123.810	0.891	-164.190
2100	0.958	-161.170	1.504	-10.270	0.005	-118.200	0.892	-166.140
2150	0.958	-159.840	1.456	-12.210	0.005	-112.740	0.893	-168.060
2200	0.957	-158.560	1.412	-14.130	0.005	-108.460	0.894	-169.840
2250	0.957	-157.160	1.372	-16.010	0.005	-103.840	0.896	-171.610
2300	0.955	-155.870	1.334	-17.870	0.005	-99.310	0.896	-173.260
2350	0.954	-154.510	1.300	-19.700	0.005	-95.360	0.897	-174.830
2400	0.953	-153.120	1.268	-21.510	0.005	-91.030	0.898	-176.390
2450	0.953	-151.730	1.238	-23.250	0.005	-87.460	0.899	-177.840

(continued)

Table 7. Common Source S-Parameters ($V_{DD} = 28 \text{ Vdc}$, $I_{DQ} = 50 \text{ mA}$, $T_A = 25^\circ\text{C}$, 50 Ohm System) (continued)

f MHz	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	S ₁₁	$\angle \phi$	S ₂₁	$\angle \phi$	S ₁₂	$\angle \phi$	S ₂₂	$\angle \phi$
2500	0.952	150.340	1.211	-25.120	0.006	84.160	0.899	-179.270
2550	0.950	149.010	1.187	-26.920	0.006	80.780	0.897	179.420
2600	0.949	147.380	1.166	-28.650	0.006	77.880	0.897	178.120
2650	0.948	145.920	1.144	-30.420	0.007	74.670	0.898	176.840
2700	0.944	144.200	1.121	-32.310	0.007	71.360	0.896	175.480
2750	0.944	142.790	1.105	-34.230	0.007	67.980	0.897	174.060
2800	0.943	141.020	1.088	-36.000	0.007	63.950	0.897	172.930
2850	0.941	139.410	1.073	-37.870	0.007	61.230	0.896	171.630
2900	0.940	137.640	1.058	-39.760	0.008	59.810	0.896	170.330
2950	0.938	135.900	1.045	-41.680	0.008	58.280	0.896	169.040
3000	0.937	133.860	1.032	-43.610	0.008	56.740	0.895	167.510

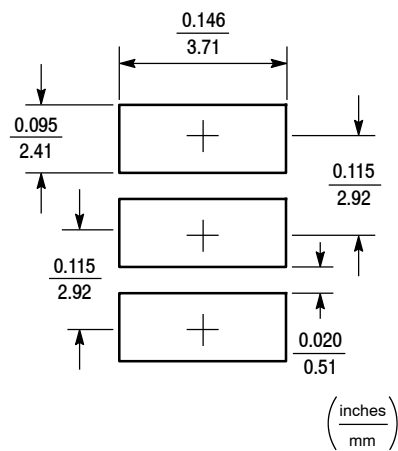
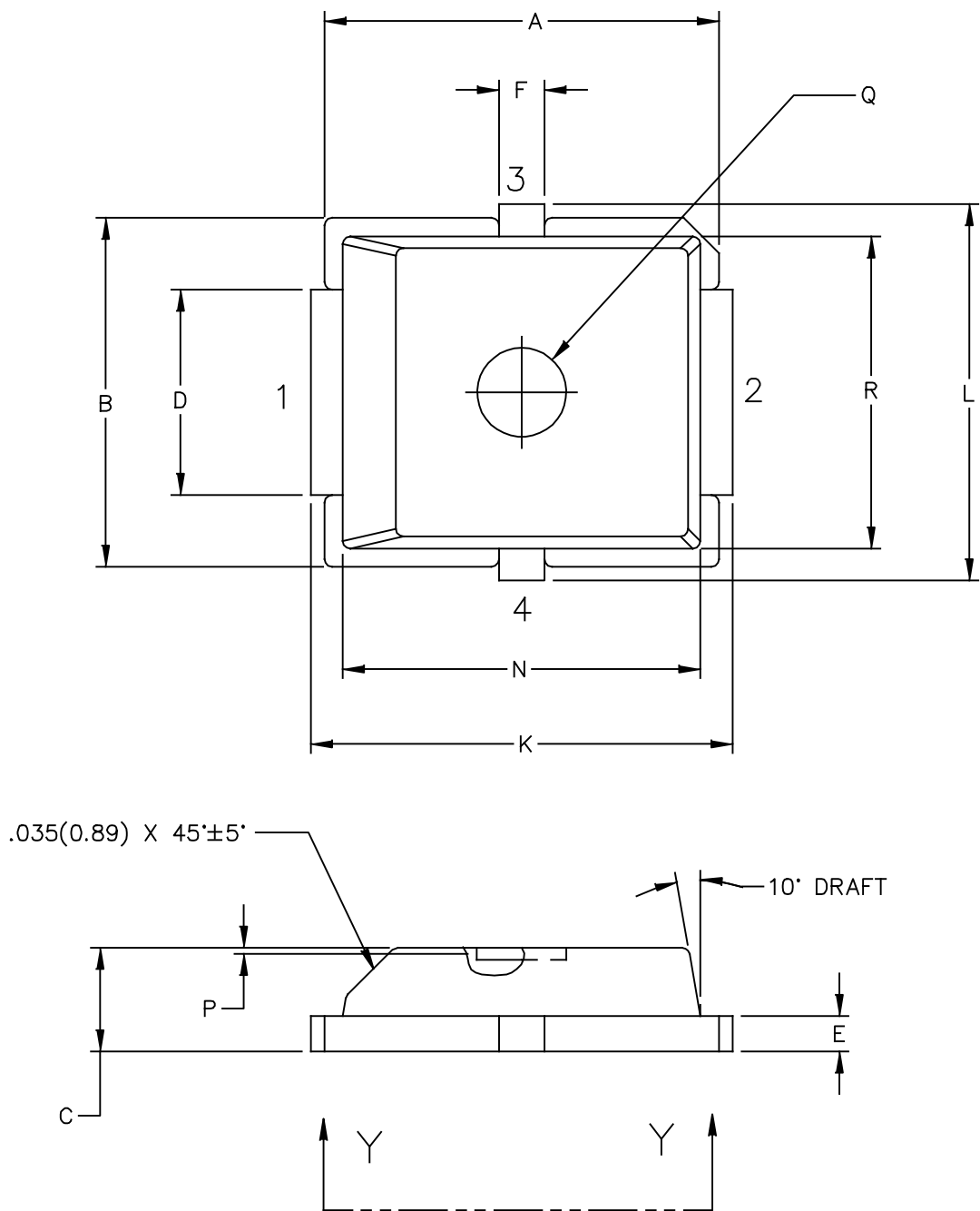


Figure 14. Solder Footprint for PLD-1.5

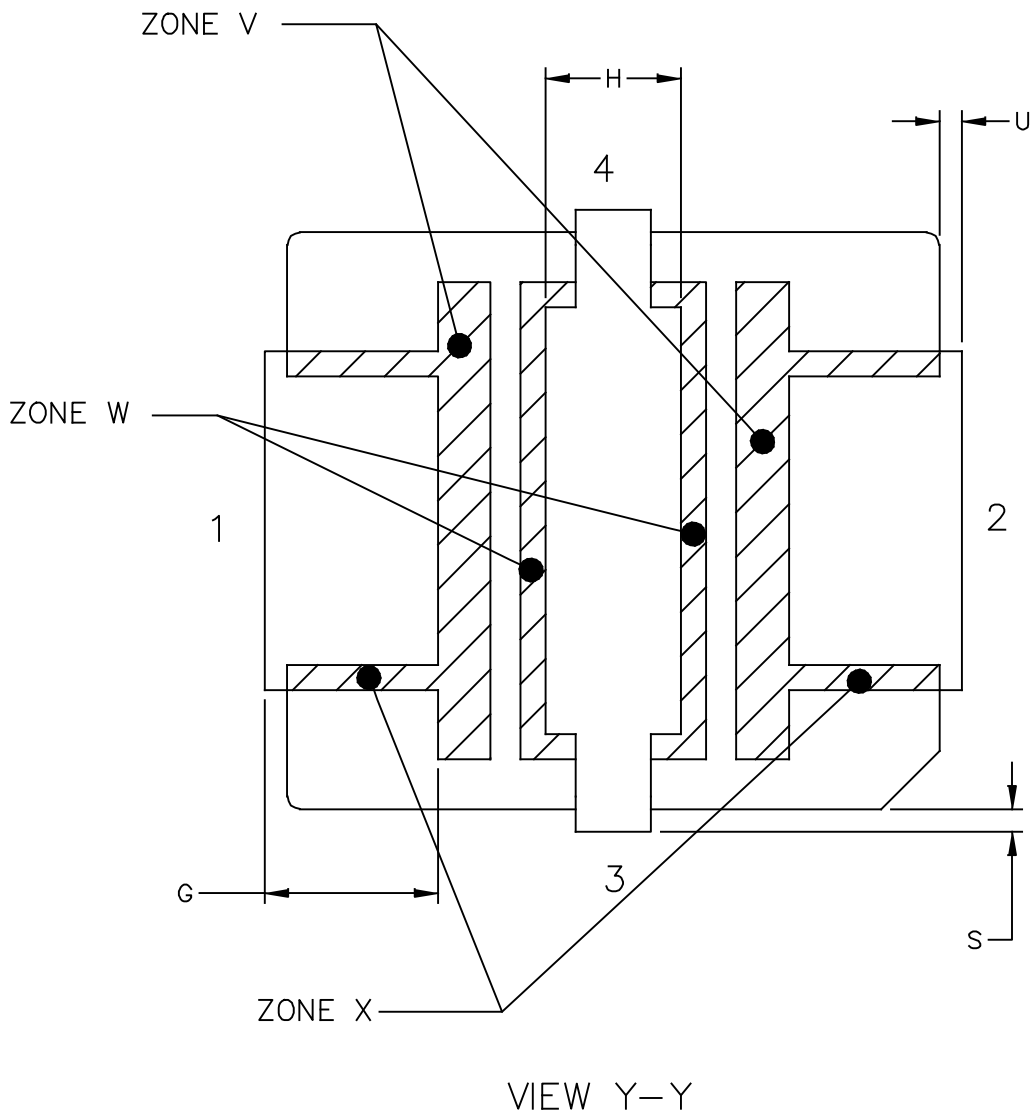


Figure 15. Product Marking

PACKAGE DIMENSIONS



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TITLE: PLD-1.5		DOCUMENT NO: 98ASB15740C	REV: D
		CASE NUMBER: 466-03	31 MAR 2005
		STANDARD: NON-JEDEC	



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TITLE: PLD-1.5		DOCUMENT NO: 98ASB15740C		REV: D
		CASE NUMBER: 466-03		31 MAR 2005
		STANDARD: NON-JEDEC		

NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. RESIN BLEED/FLASH ALLOWABLE IN ZONES V, W AND X.

STYLE 1:

PIN 1 – DRAIN
 PIN 2 – GATE
 PIN 3 – SOURCE
 PIN 4 – SOURCE

INCH			MILLIMETER		INCH			MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
A	.255	.265	6.48	6.73	Q	.055	.063	1.40	1.60
B	.225	.235	5.72	5.97	R	.200	.210	5.08	5.33
C	.065	.072	1.65	1.83	S	.006	.012	0.15	0.31
D	.130	.150	3.30	3.81	U	.006	.012	0.15	0.31
E	.021	.026	0.53	0.66	ZONE V	.000	.021	0.00	0.53
F	.026	.044	0.66	1.12	ZONE W	.000	.010	0.00	0.25
G	.050	.070	1.27	1.78	ZONE X	.000	.010	0.00	0.25
H	.045	.063	1.14	1.60					
J	.160	.180	4.06	4.57					
K	.273	.285	6.93	7.24					
L	.245	.255	6.22	6.48					
N	.230	.240	5.84	6.10					
P	.000	.008	0.00	0.20					
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TITLE: PLD—1.5					DOCUMENT NO: 98ASB15740C			REV: D	
					CASE NUMBER: 466—03			31 MAR 2005	
					STANDARD: NON—JEDEC				

PRODUCT DOCUMENTATION AND SOFTWARE

Refer to the following resources to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator

For Software, do a Part Number search at <http://www.freescale.com>, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	July 2014	• Initial Release of Data Sheet

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